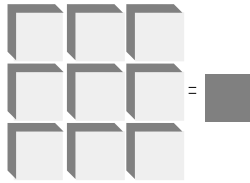




LSI/CSI



LS7082N1

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QUADRATURE CLOCK CONVERTER

April 2009

FEATURES:

- x1, x2 and x4 mode selection
- Up to 16MHz output clock frequency
- INDEX input and output
- UP/DOWN indicator output
- Programmable output clock pulse width
- On-chip filtering of inputs for optical or magnetic encoder applications.
- TTL and CMOS compatible I/Os
- +3V to +12V operation (VDD - VSS)
- **LS7082N1** (DIP); **LS7082N1-S** (SOIC) - See Figure 1

DESCRIPTION:

The **LS7082N1** is a CMOS quadrature clock converter. Quadrature clocks derived from optical or magnetic encoders, when applied to the A and B Inputs of the **LS7082N1**, are converted to strings of Up Clocks and Down Clocks. Pulses derived from the Index Track of an encoder, when applied to the INDX input, produce absolute position reference pulses which are synchronized to the Up Clocks and Down Clocks. These outputs can be interfaced directly with standard Up/Down counters for direction and position sensing of the encoder.

INPUT/OUTPUT DESCRIPTION:

VDD (Pin 1)

Supply Voltage positive terminal.

INDX (Pin 2)

Encoder Index pulses are applied to this input.

RBIAS (Pin 3)

Input for external component connection. A resistor connected between this input and Vss adjusts the output clock pulse width (Tow). For proper operation, the output clock pulse width must be less than or equal to the A, B pulse separation (Tow - Tps).

Vss (Pin 4)

Supply Voltage negative terminal.

A (Pin 5)

Quadrature Clock Input A. This input has a filter circuit to validate input logic level and eliminate encoder dither.

x2 (Pin 8)

A low level applied to this input selects x2 mode of operation. See Table 1 for Mode Selection Truth Table and Figure 2 for Input/Output timing relationship.

B (Pin 9)

Quadrature Clock Input B. This input has a filter circuit identical to input A.

PIN ASSIGNMENT - TOP VIEW

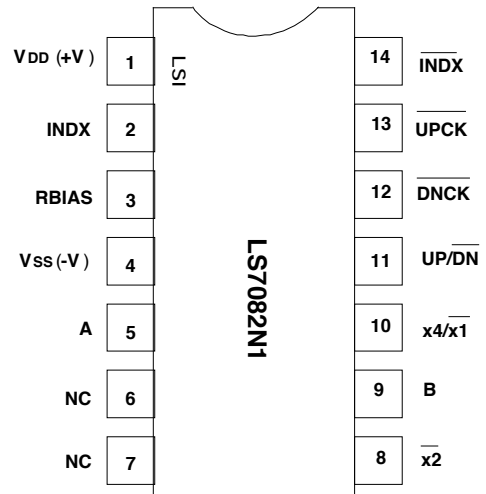


FIGURE 1

TABLE 1. MODE SELECTION TRUTH TABLE

x2 Input	x4/x1 Input	MODE
0	0 or 1	x2
1	0	x1
1	1	x4

x4/x1 (Pin 10)

This input selects between x1 and x4 modes of operation. See Table 1 for Mode Selection Truth Table and Figure 2 for Input/Output timing relationship.

UP/DN (Pin 11)

The count direction at any instant is indicated at this output. An UP count direction is indicated by a high, and a DOWN count direction is indicated by a low (See Figure 2).

DNCK (Pin 12)

This DOWN Clock output consists of low-going pulses generated when A input lags the B input (See Figure 2).

UPCK (Pin 13)

This UP Clock output consists of low-going pulses generated when A input leads the B input (See Figure 2).

INDX (Pin 14)

This output consists of low-going pulses generated by a positive clock transition at the A input when INDX input is high and B input is low and a negative clock transition at the B input when INDX input is high and A input is high. (See Figure 2).

NOTE: All unused input pins must be tied to VDD or Vss.

ABSOLUTE MAXIMUM RATINGS:

PARAMETER	SYMBOL	VALUE	UNITS
DC Supply Voltage	VDD - VSS	16.0	V
Voltage at any input	VIN	VSS - 0.3 to VDD + 0.3	V
Operating temperature	TA	0 to +85	°C
Storage temperature	TSTG	-55 to +150	°C

DC ELECTRICAL CHARACTERISTICS:

(All voltages referenced to VSS, TA = 0°C to 85°C.)

PARAMETER	SYMBOL	MIN	MAX	UNITS	CONDITION
Supply voltage	VDD	3.0	12.0	V	-
Supply current	IDD	-	20	μA	VDD = 12V, All input frequencies = 0Hz RBIAS = 2M
x4/x1	VIL	-	0.5	V	-
x2, INDX Logic Low	VIL	-	0.3VDD	V	-
A, B Logic Low	VIL	-	0.7	V	VDD = 3V
		-	1.0	V	VDD = 5V
		-	2.8	V	VDD = 12V
x4/x1	VIH	VDD - 0.5	-	V	-
x2, INDX Logic High	VIH	0.7VDD	-	V	-
A, B Logic High	VIH	2.0	-	V	VDD = 3V
		3.0	-	V	VDD = 5V
		6.6	-	V	VDD = 12V
ALL OUTPUTS:					
Sink Current	IOL	1.3	-	mA	VDD = 3V
VOL = 0.4V		1.9	-	mA	VDD = 5V
		2.9	-	mA	VDD = 12V
Source Current	IOH	0.83	-	mA	VDD = 3V
VOH = VDD - 0.5V		1.1	-	mA	VDD = 5V
		1.6	-	mA	VDD = 12V

TRANSIENT CHARACTERISTICS:

(TA = 0°C to 70°C)

PARAMETER	SYMBOL	MIN	MAX	UNITS	CONDITION
A, B inputs: Validation Delay	TvD	-	250	ns	VDD = 3V
		-	170	ns	VDD = 5V
		-	71	ns	VDD = 12V
A, B inputs: Pulse Width	TPW	TvD + Tow	Infinite	ns	-
A to B or B to A Phase Delay	TPS	Tow	Infinite	ns	-
A, B frequency	fA, B	-	$\frac{1}{2TPW}$	Hz	-
Input to Output Delay	TDS	-	280	ns	VDD = 3V
		-	220	ns	VDD = 5V
		-	120	ns	VDD = 12V Includes input validation delay
Output Clock Pulse Width	Tow	50	-	ns	See Fig. 4 & 5

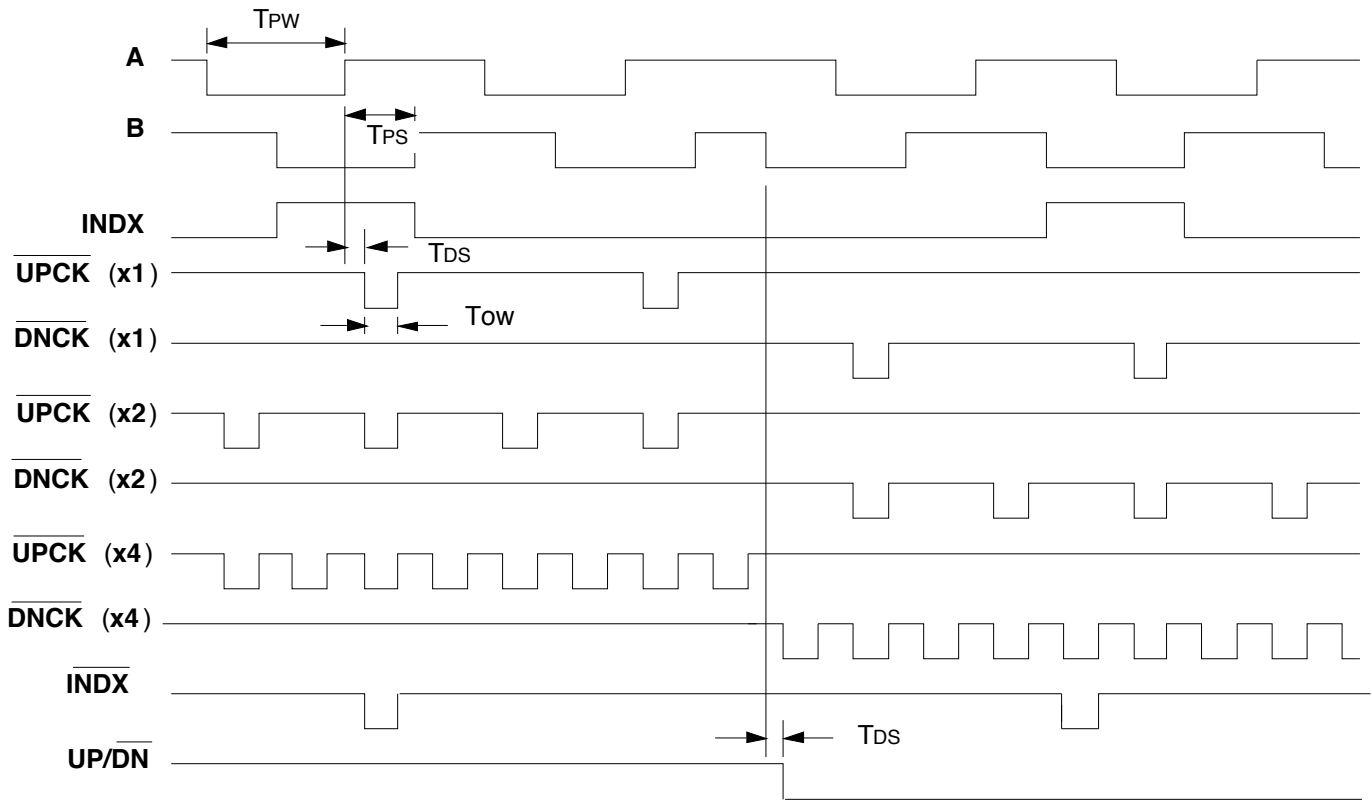


FIGURE 2. LS7082N1 INPUT/OUTPUT TIMING DIAGRAM

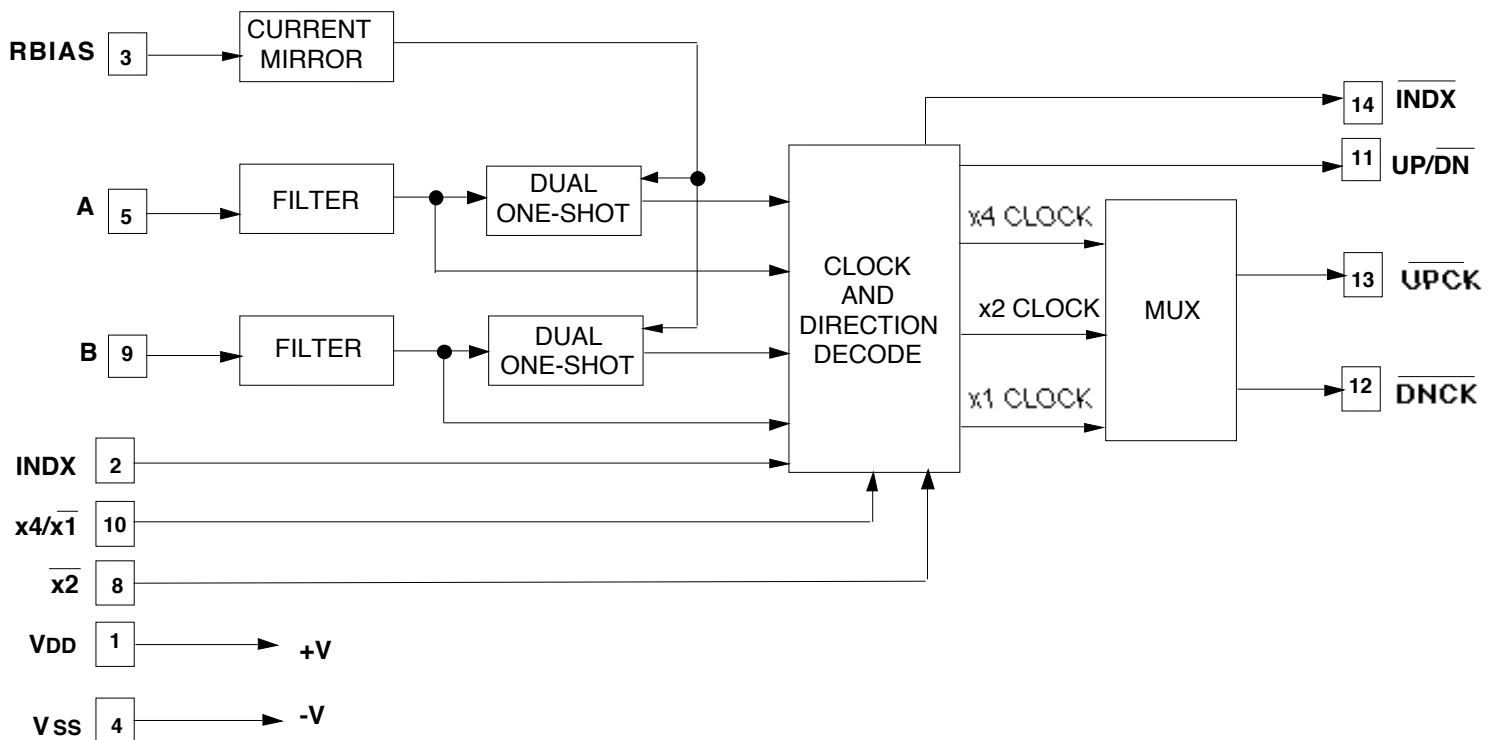


FIGURE 3. LS7082N1 BLOCK DIAGRAM

NOTE : Vertical axis is output clock pulse width, T_{ow} , ns

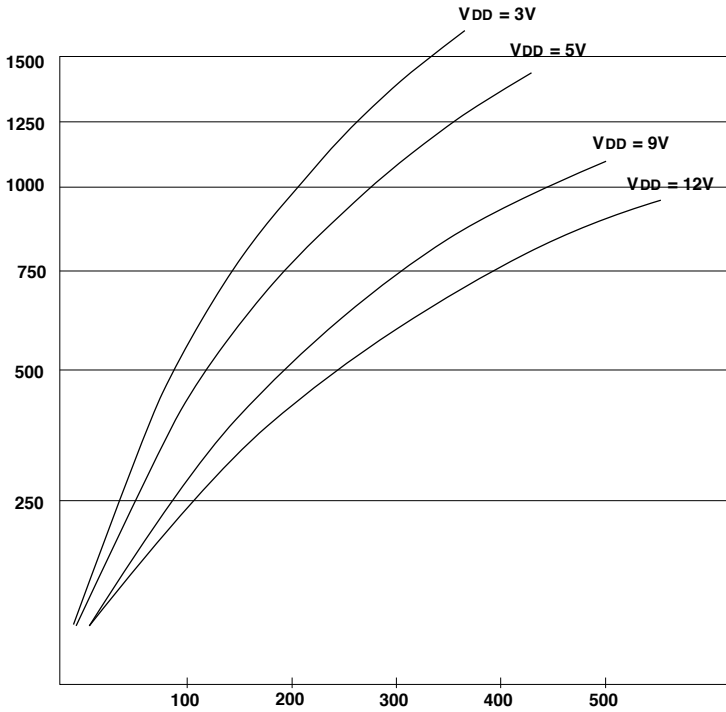


Figure 4. T_{ow} vs R_{BIAS} , k Ω

NOTE: Vertical axis is output clock pulse width, T_{ow} , μ s

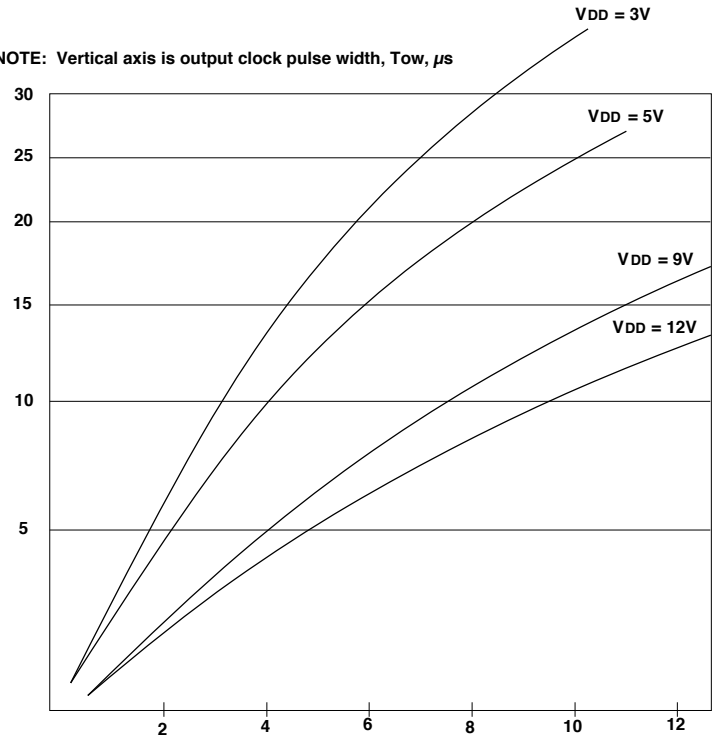


Figure 5. T_{ow} vs R_{BIAS} , M Ω

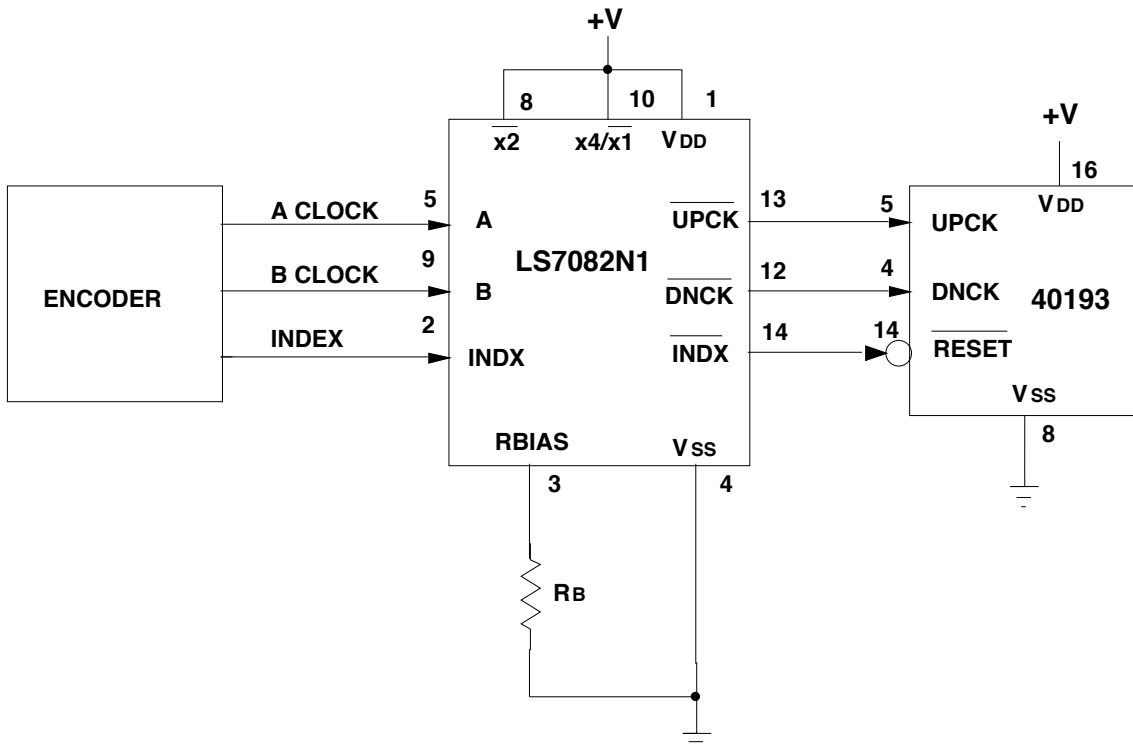


FIGURE 6. A TYPICAL APPLICATION in x4 MODE

NOTE: When driving a counter that requires \overline{CLK} and Direction input, the \overline{UPCK} and DNCK must be externally "Ored" together to generate one clock, \overline{CLK} . \overline{CLK} can be applied directly to the Clock input of counters that advance on the positive edge of the clock. If the counter advances on the negative edge of the clock, an inverter must be added between \overline{CLK} and the Clock input of the counter.

The information included herein is believed to be accurate and reliable. However, LSI Computer Systems, Inc. assumes no responsibilities for inaccuracies, nor for any infringements of patent rights of others which may result from its use.